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PAIRED CHIP PACKAGING STRUCTURE

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[There are no amendments to this patent.]

Claim

Paired chip packaging structure characterized in that, in a paired chip packaging structure wherein two or more paired chips are alternately connected and packaged on a printed wiring board,

electrode faces are formed on the top surface of one of the paired chips and on the bottom surface of the other paired chip, with a solder bump being formed on either of these electrode faces,

with the bottom surface of the aforementioned one paired chip being connected to the printed wiring board and at the same time with its top surface being made to face the bottom surface of the other paired chip, and with the aforementioned top and bottom electrode faces being connected via the aforementioned solder bump(s).

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